4. Jan. 1978

2758
LOWPOWER, +5V 1Kx8 UV EPROM

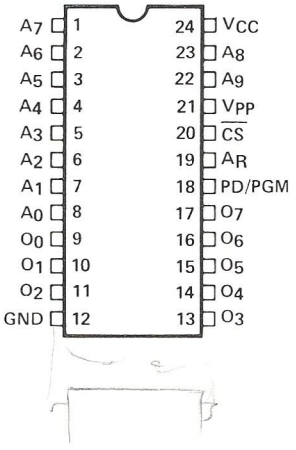
- **Single +5V Power Supply**
- **Simple Programming Requirements**
  Single Location Programming
  Programs With One 50ms Pulse
- **Low Power Dissipation**
  525mW Max Active Power
  132mW Max Standby Power
- **Fast Access Time: 450ns Max In Active and Standby Power Mode**
- **Inputs and Outputs TTL Compatible During Read and Program**
- **Three-State Outputs For or-Ties**

The Intel® 2758 is a 8192-bit ultraviolet erasable and electrically programmable read-only-memory (EPROM). The 2758 operates from a single 5V power supply, has a static power-down mode, and features fast, single address location programming. It makes designing with EPROMs faster, easier and more economical. The total programming time for all 8192 bits is 50 seconds.

The 2758 has a static power-down mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW, while the maximum standby power dissipation is only 132 mW, a 75% savings. Power-down is achieved by applying a TTL-high signal to the PD/PGM input.

A 2758 system may be designed for total upwards compatibility with Intel's 16K 2716 EPROM (see Applications Note 30). The 2758 maintains the simplest and fastest method yet devised for programming EPROMs — single pulse TTL-level programming. There is no need for high voltage pulsing because all programming controls are handled by TTL signals. Now it is possible to program on-board, in the system, in the field. Program any location at any time — either individually, sequentially, or at random, with the single address location programming.

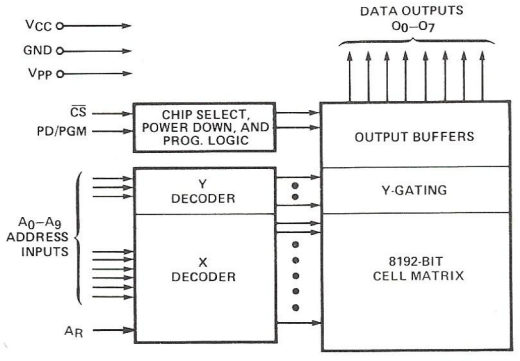
PIN CONFIGURATION



MODE SELECTION

MODE \ PINS	PD/PGM (18)	A_R (19)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Deselect	Don't Care	V_{IL}	V_{IH}	+5	+5	High Z
Power Down	V_{IH}	V_{IL}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IL}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM



PIN NAMES

A_0–A_9	ADDRESSES
PD/PGM	POWER DOWN/PROGRAM
$\overline{CS}$	CHIP SELECT
O_0–O_7	OUTPUTS
A_R	SELECT REFERENCE INPUT LEVEL

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -10°C to +80°C
Storage Temperature . . . . . -65°C to +125°C
All Input or Output Voltages with Respect to Ground . . . . . +6V to -0.3V
V_{PP} Supply Voltage with Respect to Ground . . . . . +28V to -0.3V

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

READ OPERATION

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{CC}[1,2] = +5V ±5%, V_{PP}[2] = V_{CC} ±0.6V[3]

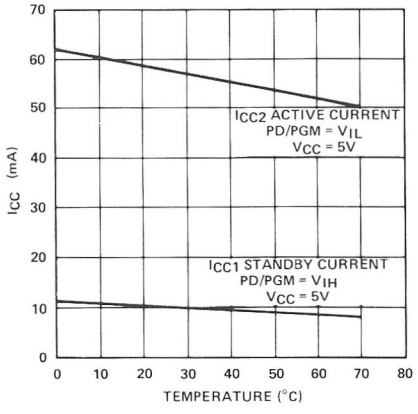
Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[4]	Max.		
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{PP1}[2]	V_{PP} Current			5	mA	V_{PP} = 5.85V
I_{CC1}[2]	V_{CC} Current (Standby)		10	25	mA	PD/PGM = V_{IH}, $\overline{CS}$ = V_{IL}
I_{CC2}[2]	V_{CC} Current (Active)		57	100	mA	$\overline{CS}$ = PD/PGM = V_{IL}
A_R[5]	Select Reference Input Level	-0.1		0.8	V	I_{IN} = 10 μA
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.2		V_{CC} + 1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA

NOTES FOR PAGES 2 AND 3:

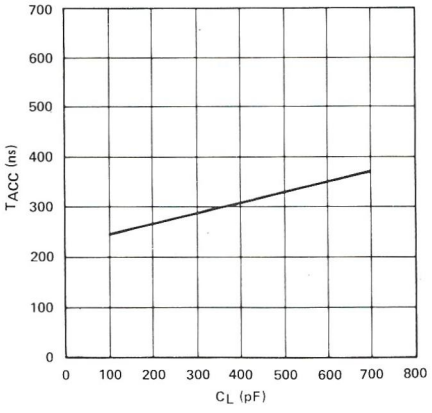
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from V_{CC} in read to 25V for programming.
4. Typical values are for T_A = 25°C and nominal supply voltages.
5. A_R is a reference voltage level which requires an input current of only 10 μA. The 2758 S1865 is also available which has a reference voltage level of V_{IH} instead of V_{IL}.
6. This parameter is only sampled and is not 100% tested.
7. t_{ACC2} is referenced to PD/PGM or the addresses, whichever occurs last.

Typical Characteristics

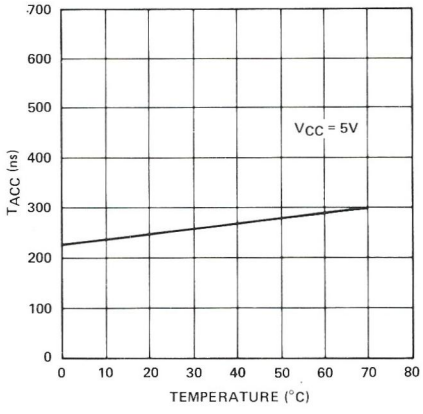
I_{CC} CURRENT vs. TEMPERATURE



ACCESS TIME vs. CAPACITANCE



ACCESS TIME vs. TEMPERATURE



A.C. Characteristics

T_A = 0°C to 70°C, V_{CC}[1] = +5V ±5%, V_{PP}[2] = V_{CC} ±0.6V[3]

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[4]	Max.		
t_{ACC1}	Address to Output Delay		250	450	ns	PD/PGM = $\overline{CS}$ = V_{IL}
t_{ACC2}[7]	PD/PGM to Output Delay		280	450	ns	$\overline{CS}$ = V_{IL}
t_{CO}	Chip Select to Output Delay			120	ns	PD/PGM = V_{IL}
t_{PF}	PD/PGM to Output Float	0		100	ns	$\overline{CS}$ = V_{IL}
t_{DF}	Chip Deselect to Output Float	0		100	ns	PD/PGM = V_{IL}
t_{OH}	Address to Output Hold	0			ns	PD/PGM = $\overline{CS}$ = V_{IL}

Capacitance[6] T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	12	pF	V_{OUT} = 0V

NOTE: Please refer to page 2 for notes.

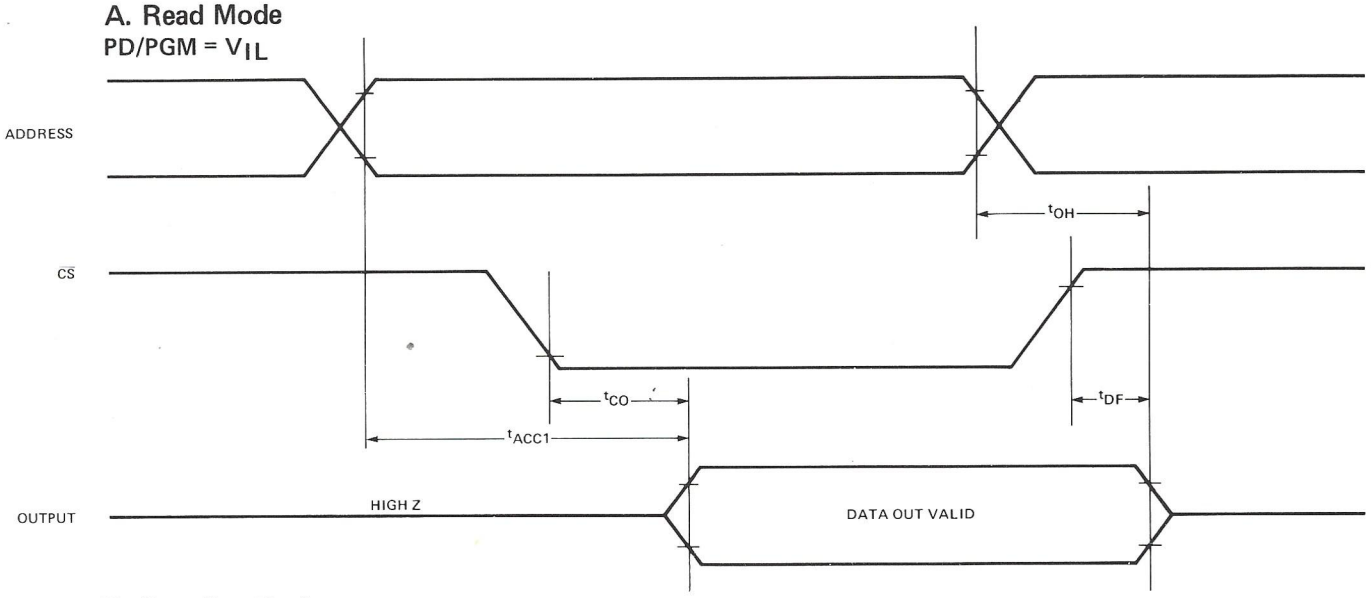
A.C. Test Conditions:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

WAVEFORMS

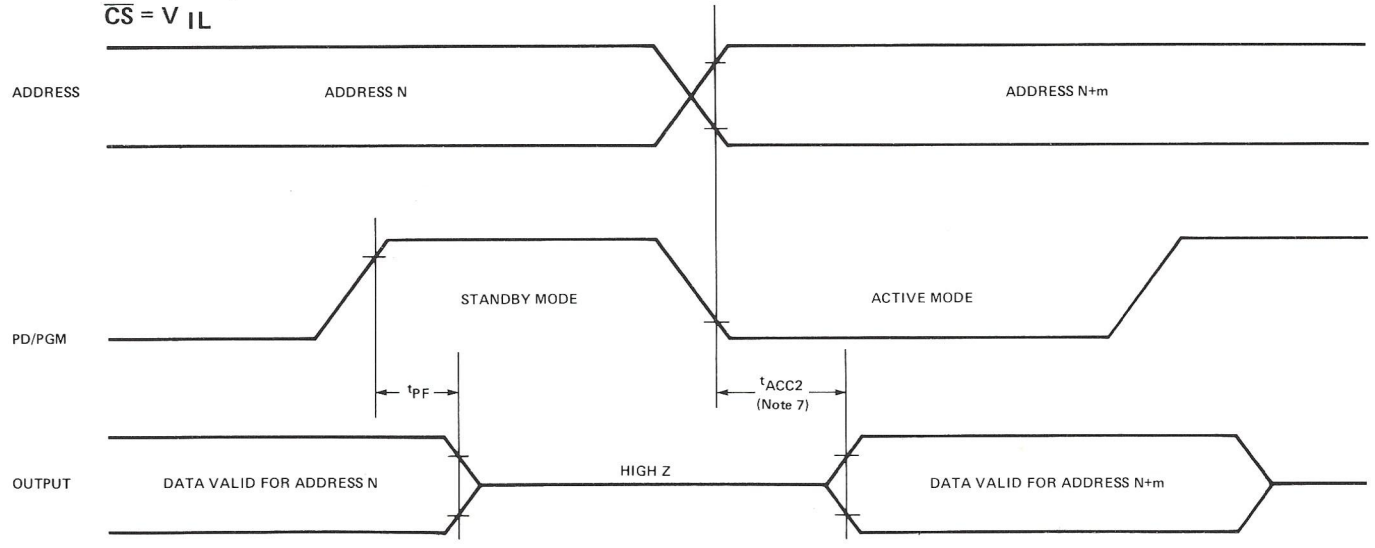
A. Read Mode

PD/PGM = V_{IL}



B. Standby Mode

$\overline{CS}$ = V_{IL}

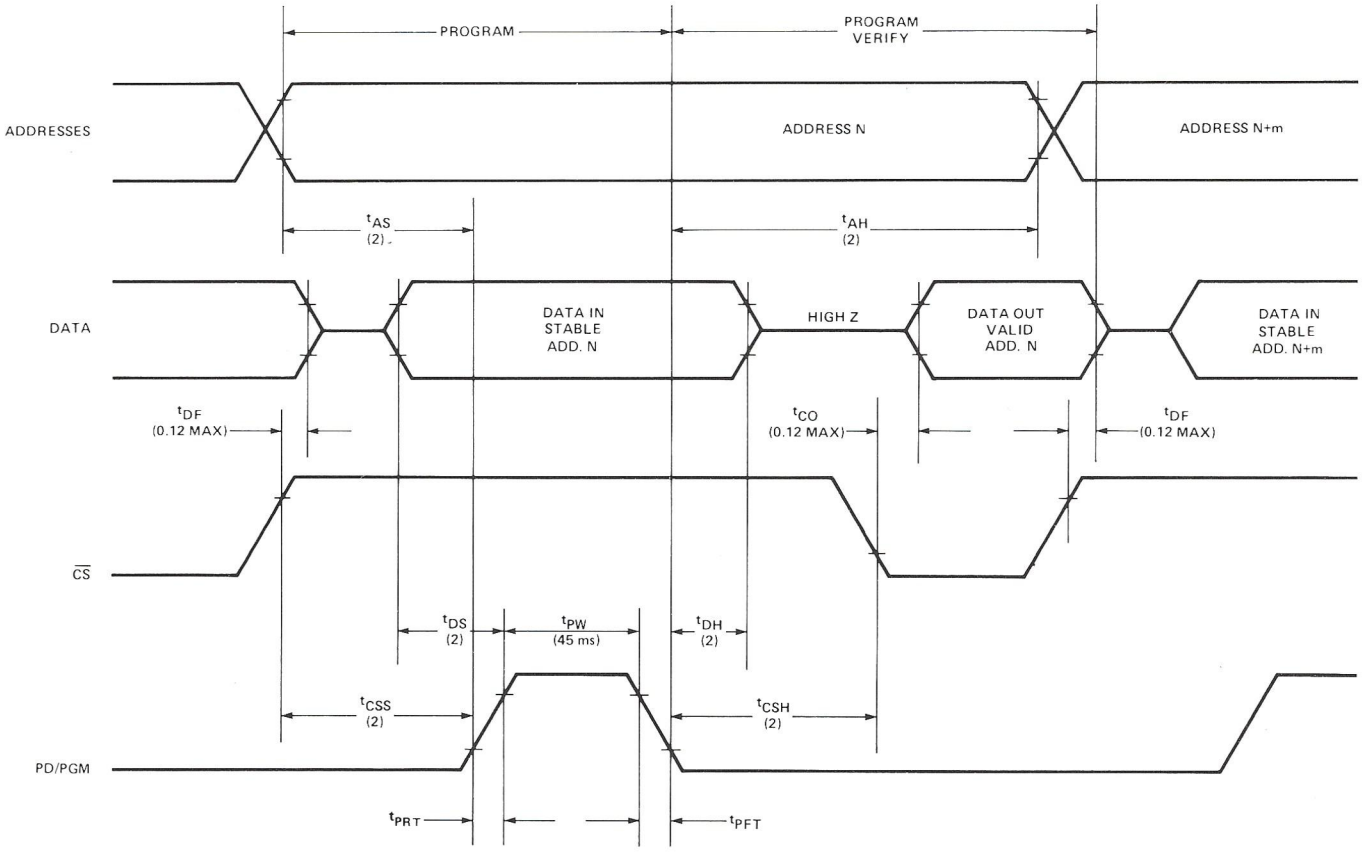


A.C. Conditions of Test:

V_{CC} . . . . . 5V ±5%	Input Pulse Levels . . . . . .0.8V to 2.2V
V_{PP} . . . . . 25V ±1V	Input Timing Reference Level . . . . . 1V and 2V
Input Rise and Fall Times (10% to 90%) . . . . . 20 ns	Output Timing Reference Level . . . . . 0.8V and 2V

PROGRAMMING WAVEFORMS

V_{PP} = 25V ±1V, V_{CC} = 5V ±5%



NOTE: ALL TIMES SHOWN IN PARENTHESES ARE MINIMUM TIMES AND ARE μSEC UNLESS OTHERWISE NOTED.

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