Design and Characterization of Time Stamping IP Core for Clock Synchronization

Muhammed Thaha
thaha.thaha007@gmail.com

***Abstract*- In today's modern network, time is becoming more and more critical than before, time synchronization is significant in many different technologies and applications like test and measurement, factory automation, power plants, robotic control, telecommunication and financial applications. Most of the communication networks are running over IP network, which is sensitive to issues in timing and synchronization. IEEE 1588 Precision Time Protocol (PTP) is a key standard for providing synchronization to networks, at high precision and provides both frequency and time synchronization, through an exchange of packets over network. Stamping PTP messages accurately in physical layer taking advantage of hardware is one of the key technologies, to achieve the objective of high precision time synchronization. This work forward, design and characterization of re-configurable and re-useable hardware time stamping unit along with a parser having L2, L4 PTP messages, compatible with PTP version1 and 2. It works independently or along with a protocol stack to achieve fractional micro second level precision. The hardware unit is synthesized with Xilinx ISE® tool implemented in virtex 6® and analyzed using Chip Scope Pro® integrated logic analyzer. It is aimed to use with high end SOC architecture as a reconfigurable and re usable IP core.**

I. INTRODUCTION

Along with the development of the electronics and electrical industry more and more electronic intelligent devices for measurement, protection and control have been put into use to improve the stability and reliability of the system. But there is also an increasing demand on accurate time synchronization for range of fields, most of the today's communication networks are running over IP network which is highly vulnerable to issues in timing and synchronization in proper running of communication network especially telecommunication networks due to highly unpredictable traffic flows, such as high-speed wireless networks that need to know the position of nodes and require precise control of devices that are used in extreme situations or high precision operations [1-2].

There are two popular methods of time precision viz; location based synchronization and frequency based synchronization. Location based method uses global position system (GPS) [3], which receives location information from satellite for synchronization and gives micro second accuracy but with an over head due to the extra antenna requirement. Frequency based synchronization uses Network Time Protocol (NTP) [4], which does not need any extra module gives only millisecond accuracy. To improve this, IEEE 1588 Time Synchronization Standard was announced in 2002 [5], as version1 and updated at 2008 [6], as version 2. IEEE 1588 is designed for spatially localized systems with options of scalability, it aims to give microsecond to sub microsecond accuracy with provision of redundant and fault tolerant system, having administration free operation and thus applicable for low end to high end and low cost devices.

IEEE 1588 is typically implemented using software-based time stamping. However, software implementation delay and jitter at the application level when packets are delivered cause problems in many cases. The best way to reduce these problems is hardware implementation of time stamping [7- 8].

PTP's operation principle is to exchange messages regularly in an interval to determine the offset between master and slave but also the message transit delay through the network. Figure 1 shows how PTP messages are exchanged. In an attempt to synchronize between two nodes, Delay and Offset should be known. Delay refers to time taken to send a message between two nodes. Offset is the real time difference between two nodes. Delay and Offset can be calculated using the following simple equation (1, 2).

$$Delay = [(t1-t2) + (t4-t3)] / 2 \quad (1)$$

$$Offset = [(t1-t2) - (t4-t3)] / 2 \quad (2)$$

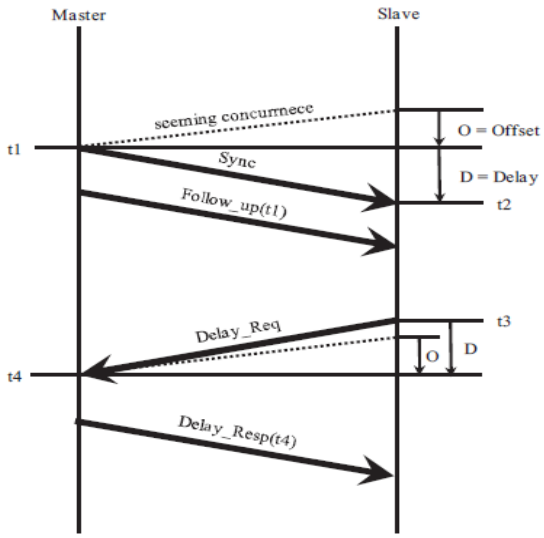


Figure 1.The Process of Synchronization

The slave clock requires four measured values, t1, t2, t3, t4, to calculate delay and offset. t1 and t3 are the send time of the Synch and Delay_Req messages, t2 and t4 are the receive time of synch and delay_req messages. t2, t3 were generated at slave side, Follow_up and Delay_Resp signals contain t1 and t4.

The PTP environment offers a verity of possible time stamp point. Stamping PTP messages accurately in physical layer taking advantage of hardware is one of the key technologies, to achieve the objective of high precision time synchronization.

This paper deals with the design and characterization of reconfigurable and reusable time stamping hardware unit suitable for both master and slave, to achieve synchronization in microsecond level precision along with protocol stack, compatible with IEEE 1588 Version1 or Version2 provides fractional microsecond range accuracy, sufficient to stamp layer 2 and layer 4. event messages with Stacked VLAN, MPLS tags and UDP IPv4 or UDP IPv6 protocols. The hard ware unit is synthesized using Xilinx ISE® tool implemented in Virtex6® FPGA analyzed using Chip Scope Pro integrated logic analyzer. This paper organized as follows, section 2: Top level FSM, section 3: Detail operation of each module, section 4: simulation and analysis results, section 5: conclusions, 6: reference.

2. Top Level FSM

Figure shows the top level finite state machine having four states: Initial state (INIT), time stamping state (STAMP), message receiving and extraction state (PARSER) and final clock offset generation state (OFFSET).

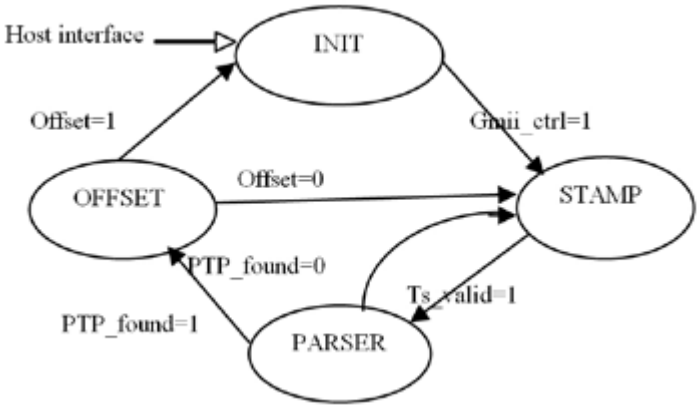


Fig2. Top Level FSM

INIT: Here provision of environment initialization by host, Offset correction of real time clock. STAMP: Time stamping for receiving, transmitting messages. PARSER: 32 bit packet parser data path checks PTP event.
OFFSET: Offset and delay are calculated using equation (1) and (2). Use software to generate the clock offset to achieve synchronization.

3. Hardware Implement

In this paper, the IEEE 1588 hardware is implemented with four modules, a Time Stamp, a Parser, a Real Time Clock and a Host Interface. Figure 3 shows Top Level architecture.

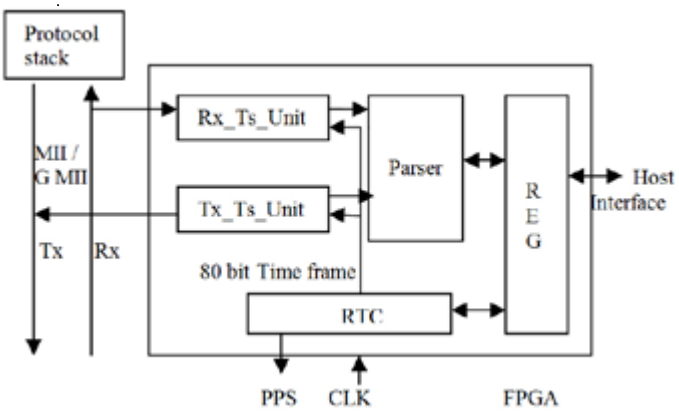


Fig3. Top Level Block Diagram

A. Time Stamp

Separate Time Stamp module for receiver and transmitter, one end connected to the MII or GMII interface, by using giga mode signal we can switch input data mode. Every cycle real time clock outs 80 bit time frame to the Time Stamp unit. Message arrival indicated by start delimiter, it enable time stamping. Then rise valid signal for converting 8 bit data packets to 32 bit data packets by using a data gear box.

B. parser

Parser operates on 32 bit packet size of receiving data, parser have chunk counter, it extract the receiving data entry details belongs to different protocols layer and allows the extractor to check the condition for different stratagem to find out PTP event message. If it satisfied, raise PTP_found high. Then extract 4bit PTP_Message_Id, 12 bit PTP_Sequence_Id and 16 bit PTP_Check_sum are combined to form 32 bit PTP Information. This PTP Information and Time Stamp of 80 bits are writing to receiver or transmitter FIFO. If parsed message is not a PTP event, then burst the Time Stamp and prepare to collect other message.

C. Real Time Clock

It receives input from the system clock and generate 80 bit Time of day (TOD), one pulse per second output. 80 bit include 48 bit second and 32 bit nanosecond field. Direct time adjustment set up, frequency set up for drift compensation and precise time adjustment with a small time mark these are the facilities provided in RTC for adjusting clock offset with slave and master, RTC have a power of 2^48 second time period. After computation of offset by software stack update the system Clock, this process repeat until the slave synchronized with master

D. Host Interface

A set of 64 slice registers ordered as 32 bit in each slice offer the host interfaces, it situate environment through update registers and drive the hardware unit in different mode with control registers, these are possible by using protocol stack or software driver.

Key Points in Implementation

PTP system with the best performance, to ensure the following:

- All PTP nodes in the entire domain use the same transport protocol.
- All PTP nodes in the entire domain use the same Best Master Clock algorithm.
- All nodes in the domain use the same status configuration items.
- All nodes in the domain use the same delay measurement mechanism.
- The attributes and configurable data set members of all nodes in the system use the same default values.
- The attributes of all nodes in the system have the same value range, that is, the same maximum and minimum values.
- All nodes in the domain use the same PTP template.
- All nodes in the domain use the same PTP version.

Feature Description

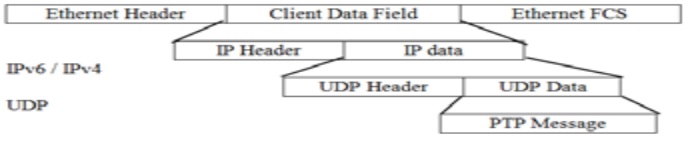
RTC: Real Time Clock.

- Standard PTP clock output with 2^48 second and 2^32 nanosecond time format.
- Tunable accumulator based clock with 2^-8 and 2^-32 nanosecond time resolution period resolution.
- Direct time write, with 2^-8 nanosecond resolution.
- Direct frequency write, with 2^-32 nanosecond resolution.
- Timed temporary time adjustment, with 2^-8 nanosecond resolution and 32bit timer.
- Variety of input clock frequencies.
- Clock Domain crossing hand-shaking, for SW read and write access.

TSU: Time Stamping Unit.

- Two-Step PTP operation.
- GMII interface monitor with line-speed PTP packet parsing.
- Varieties of PTP packet formats are supported, in this fashion: Layer 2 PTP packets with stacked VLAN tags, IPv4 UDP or IPv6 UDP PTP packet with stacked VLAN tags or stacked MPLS labels.
- Configurable 8bit mask to selectively timestamp PTP event packet based on message type values, in this manner; 0: Sync, 1: Delay_Request, 2: Pdelay_Request, 3: Pdelay_Response, 4 to 7: Reserved for future PTP event message types
- 32 bit packet parser data path for easier timing closure.
- 15-entry timestamp queue with each entry is 128 bit; consist of 80 bit timestamp, 32bit packet identity data field and 16 bit extra information.
- Time stamping for receiving and transmitting message uses same procedure. Thus ingress and egress delays of time Stamping unit is equal and opposite, this improve symmetry of the network.

Input Vector



Bits								Octets	Offset
7	6	5	4	3	2	1	0		
PCAP header								20	0
Layer 2 / 4 C-VLAN								4	4
Layer 2 PTP mask/Layer 4 MPLS								4	5
Layer 4 IPv4/IPv6								16	6
Layer 4 UDP								4	7
Layer 4 PTP mask								4	8
PTP message								10	10

Table 1: PTP message format

Table1; shows the organization of input message for layer 2 and layer 4 by stacking VLAN or MPLS and UDP with IPv4 or UDP with IPv6 protocols. Input message received from gmii or mii interface but parser unit operates on 32 bit packets. First 5 packets are PCAP header next 7 packets are used to set layer 2 or layer 4 and Packets above 14 include PTP node information's.

4. Result of Simulation

Figure4, Shows the important case of time stamping and event message detection

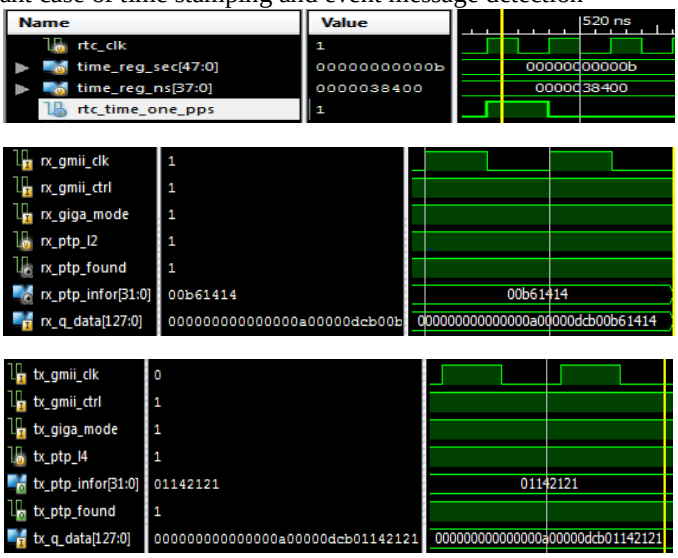


Fig4. Simulation Result

Received message is Network Layer 2 event message having message id=0 (synchronous message), check sum=0B6, sequence id =1414. Transmitted message is Network Layer 4 IPv4 UDP Event message having message id=0 (synchronous message), check sum=114, sequence id=2121.Transmitter or receiver time stamp field is 128 bit first 80 bit is time stamp, 32 is PTP message information and remaining 16 bit extra information

Logic Analyzer Result

Figure5, shows the Chip Scope Pro integrated logic analyzer result of time stamping and event message detection.

Bus/Signal	X	O
rtc_time_ptp_ns	2995BC16	2995BE5E
rtc_time_ptp_sec	000000000037	000000000037
rx_ptp_l2	1	1
rx_ptp_l4	0	0
rx_ptp_found	1	1
rx_q_data	00000000000000372995B9B600B61414	00000000000000372995B9B600B61414
rx_ptp_infor	00B61414	00B61414
tx_ptp_l2	0	0
tx_ptp_l4	1	1
tx_ptp_found	1	1
tx_ptp_infor	0C902121	0C902121
tx_q_data	00000000000000361BC6FE4E0C902121	00000000000000361BC6FE4E0C902121

Figure5.Result of Logic Analyzer

Received message is Network Layer 2 event message having message id=0 (synchronous message), check sum=0B6, sequence id=1414 and 80 bit time stamp field having seconds=37sec, nanoseconds=2995B9B6nsec. Transmitted message is Network Layer 4 IPv4, UDP event message having message id=0 (synchronous message), Check sum=C90, sequence id=2121 and 80 bit time stamp field having seconds=36sec, nanoseconds=1BC6FE4E nsec. Transmitter or receiver data field is 128 bit, lower 32bit is PTP message information next 80 bit field is time stamp.

5. Conclusion

IEEE 1588 is the key protocol to providing synchronization through exchange of packets over network Objective of hardware implement is high precision. Designing hardware that implements entire IEEE 1588 is rather complex. This paper refers design and characterization of re configurable and re usable hardware assisted time stamping module in Xilinx Vertex 6® FPGA with provision of software development, it works along with the protocol stack to achieve synchronization in fractional microsecond precision. Time stamping messages in between physical and data link layer with gmii or mii interface. To improve the symmetry of network, time stamping of receiving and transmitting messages uses same procedure. Each module is designed with IEEE 1364 Verilog HDL and synthesized using Xilinx ISE® tool. It is aimed to use with high end SOC architecture as re usable IP core.

Acknowledgements

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6. Reference

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