

Photovoltaic Output Stabilization with Boosting Circuit

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Abstract—This paper presents a practical DC-to-DC boost converter augmented to a photovoltaic (PV) system capable of producing a stable output voltage of $12\pm 1V$. Using commercially available parts, a PCB model of the boost converter was implemented and tested yielding gains up to 3.5 V/V and power efficiencies as high as 63%. The conclusions from these experiments were then used to evaluate the adjustments needed to be made in parameters considered in three IEEE standards 1013-2007, 1361-2003 and 1562-2007. It was determined that the number of cells required to achieve the desired voltage output can be reduced by a factor of three with the addition of the boosting circuit.

Index Terms—Photovoltaic system, boost converter, voltage stabilization.

I. INTRODUCTION

THE objective of this project was to develop and build a cost-effective model for a DC-to-DC voltage boosting circuit emulating novel components for use in alternate energy applications. The impact of the addition of this circuitry to the photovoltaic (PV) system is also considered with respect to three IEEE standards, 1562-2007, 1013-2007 and 1361-2003. The project oversaw the early stages of development through modelling and testing of the projected end-product parameters using discrete surface mount components on a PCB, and further designed and implemented key electrical components that make up the passive elements of the micro-scale boosting circuit.

We examine the low voltage amplification of a PV system such that the input voltage never exceeds the voltage seen at the output of the circuit. For this reason, of the three known DC-DC topologies, the buck, boost and buck-boost converter, the boost converter was chosen since it provides a theoretical gain range of 1 to 4 V/V [1], thus meeting the aforementioned conditions.

Here we elucidate the design concepts of the boost converter and the conclusions that can be drawn from its experimental implementation, the programming principles of the PWM generator and finally the applications to IEEE standards.

II. DESIGN PRINCIPLES

The PV system in its totality consists of the PV array itself, followed by the boosting circuit and the load output represented as a 12V operating LED display, modeling nominal rechargeable battery values. This system becomes a closed-loop system with the introduction of a negative feedback controller which dictates the duty cycle of the PWM generator supplied to the switch (Fig.1). The boost converter is a device which takes advantage of the characteristic voltage

spiking exhibited by an inductor when the current being passed through it is rapidly changed [2]. Additional features of the boost converter which this project takes advantage of are: its ability to amplify DC to DC voltage directly and the ease by which this gain characteristic can be altered with a modification in the device's switching duty cycle.

There are four key components that comprise a boost converter; the inductor, a switching transistor to throttle current through the inductor, a diode to isolate the inductor from the load during the 'charging phase,' and a capacitor to smooth the resulting boosted voltage at the output (Fig.2). The parameters for especially the active components were determined such that circuit's efficiency and size, and the microcontroller's duty cycle capabilities were optimized. Thus, to maximize the efficiency of the boost converter as well as emulate the performance of the ideal switch, transistors featuring low threshold voltages and low on-state resistances were chosen for the circuit; Schottky diodes were also selected with low forward voltages in mind. Secondly, inductance values had to be minimized, given the size restrictions inherent to integrated circuit design. To do this, the switching frequency of the boost converter was maximized. However, the third issue was due to a restriction in the resolution of duty cycles (the number of discrete duty cycles) the microcontroller can provide which is related to the switching frequency. Very high frequencies limited this resolution, making voltage stabilization much more challenging. Balancing this need for both high frequency switching for the sake of inductor compactness and higher duty cycle resolution for voltage control was one of the challenges of this project.

III. DISCRETE MODEL IMPLEMENTATION

A. Final Circuit Design and Execution

Minimization of the size of the overall device was inspired by observations of starkly improved results in device performance between breadboard and initial PCB implementations in previous phases of the project. An important aspect of this was the use of surface mount components, such as the 44-TQFP model of the selected PIC18 microcontroller. Throughout the project trace layouts were repeatedly compressed, all in an attempt to minimize line capacitances and better fit the practical duty cycle-gain curve to its theoretical maximums.

It was decided that a switching frequency of 2MHz would be implemented in this project. This particular frequency offered the best balance of low inductance and reasonable duty cycle resolution [3]. It also seemed to have the least transmission line capacitance issues, optimizing overall performance and predictability.

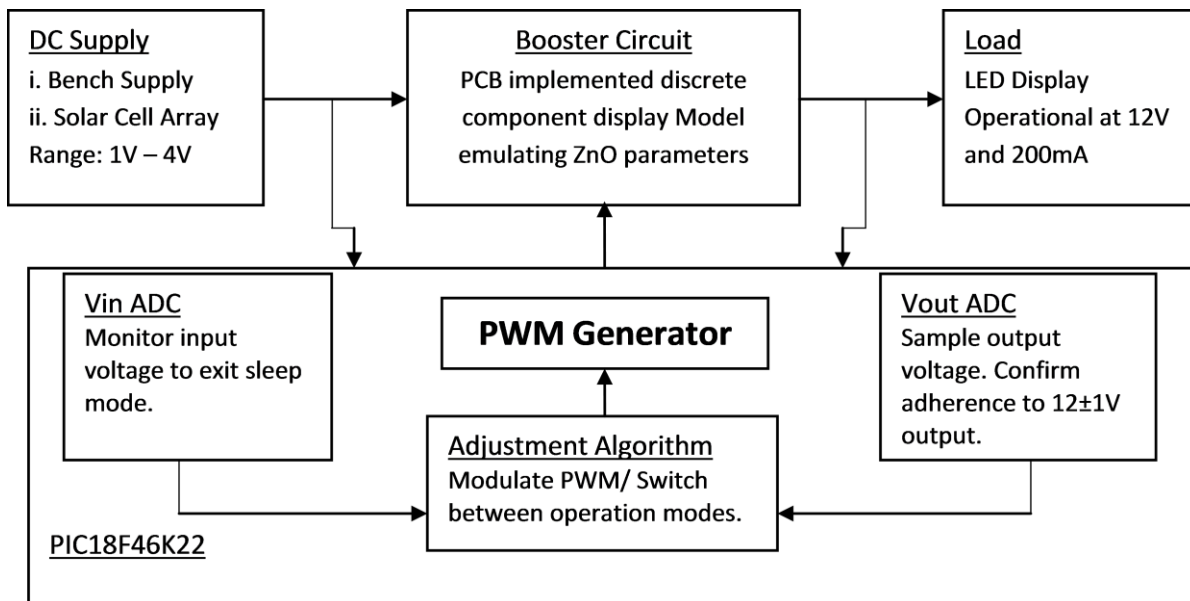


Fig. 1. Block diagram of major components of the boost converter for energy harvesting.

In order to realize voltage stabilization at the output, a feedback loop was devised using the microcontroller's analog to digital converter (ADC) features to implement a programmable gain control system. At the same time, a second ADC was used to enable the development of sleep-wake modes of operation, to assist in the preservation of power when insufficient input voltage is available to achieve desired output performance. When operated with the final revision of the microcontroller code, the device was successfully able to maintain an output voltage of $12 \pm 1V$, and both enter and exit sleep modes when input voltage fell below and returned above 3.5V respectively. This is further discussed in subsection III.B

B. Programming

The purpose of the project's code was to provide a self-regulating PWM wave input to the boost converter's switching transistor which maintains some output voltage given a variable input voltage. Code implementation takes advantage of the C-compiler native to the PIC18 family of microcontrollers, which contained functions critical to the operation of the program. As shown in the following pseudo code flow chart (Fig.3), in the active (wake) mode, the program recursively samples the voltage at the output of the device, periodically confirming that the desired output of 12V is being produced. In the event that there is a deviation from the allowed $\pm 1V$ range, the code will then attempt to return to within the allowed range by altering the duty cycle of PWM wave which controls the switching of the device transistor. Should the device reach the boundaries of the effective duty cycles which the project's microcontroller can provide, and remains unable to achieve the desired output, the device will discontinue operation in favour of sleep mode. In the case where too little voltage being produced, this prevents the device from wasting energy in futile activities, while in the less likely scenario where too much voltage is available this potentially prevents damage to the load the boost converter is

connected to. Once in sleep mode, the device will periodically sample the input voltage available from the device source, returning to sleep until a suitable voltage is available to resume operation.

*Wake mode operates the device at a 64MHz clock

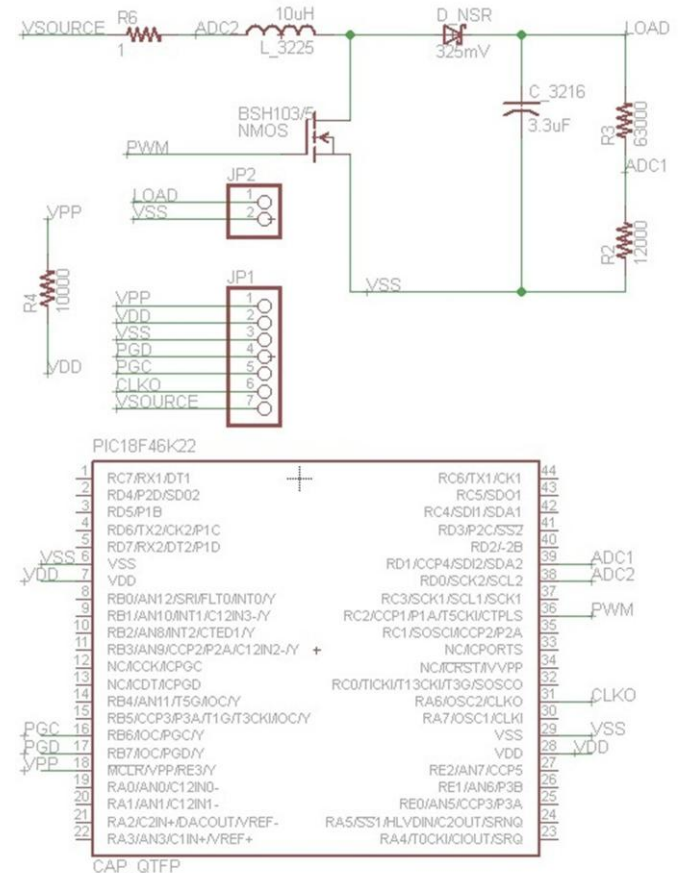


Fig. 2. Boost converter schematic with PIC18F47K22 microcontroller.

frequency, and features an enabled ECCP channel to support the PWM needed for switching control. The ADC used monitor V_{out} is reinitialized, while the ADC for V_{in} is deactivated. When returning to the wake state from sleep, the duty cycle is reset to the mid-range value 0×07 . Of note is the fact that the boundary condition check must fail five consecutive times before the sleep mode is enacted.

** Sleep mode operates the device at 31.25kHz clock frequency, which has the advantage of both lessening the number of CPU reactivations per hour to re-set counters, as well as reducing the voltage requirement for operation of the microcontroller from 3.0V to 1.8V. Sleep mode also reduces current requirements to the $10\mu\text{A}$ range. The V_{out} ADC is deactivated in this mode, as is the ECCP channel, while the V_{in} ADC is activated.

Interrupts are used to notify the microcontroller when the ADCs are finished converting, and to wake the device upon

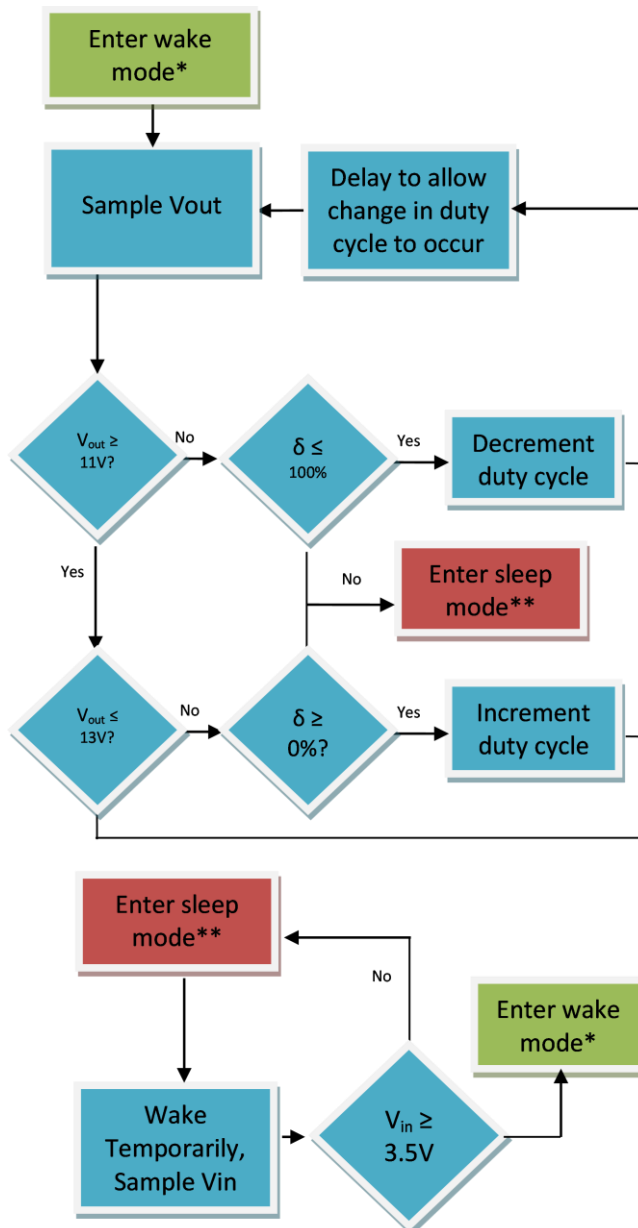


Fig. 3. Programming process flow for PWM generator.

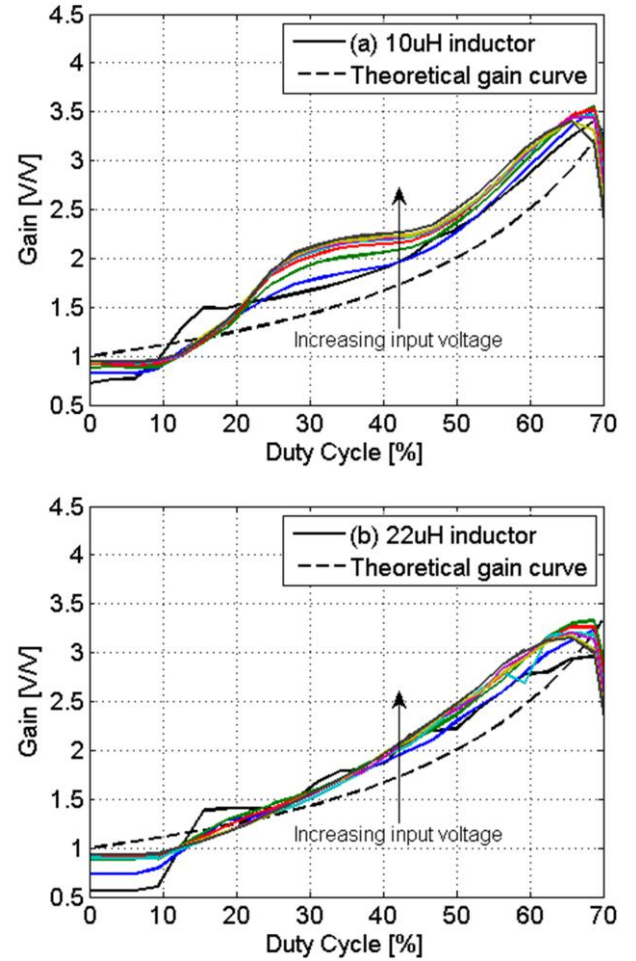


Fig. 5. Gain measurements with demonstration model with (a) $10\mu\text{H}$; and (b) $22\mu\text{H}$ inductor.

timer1 overflow.

One further modification to the code was considered for implementation: the capability of the device to optimize power efficiency by preferentially selecting duty cycles with minimal power losses; the impetus for this will be explained in subsection III.C.

C. Testing and Performance Optimization

The specifications of interest were the volt to volt gain of the boost converter under varying light intensities and duty cycle values and also the power efficiency of the system. The volt to volt gain test was performed varying an input voltage from 0.5V to 4V and at programmed duty cycles steps 3.125. The results confirmed that the gain was relatively consistent between the various input voltages.

The resulting gains were slightly higher than the expected theoretical boost converter gain given by:

$$\text{Gain} = 1/(1 - \text{Duty Cycle}) \quad (1)$$

In an attempt to optimize the voltage gain to the theoretical curve, the inductor was changed from $10\mu\text{H}$ to $22\mu\text{H}$. While this did improve the adherence to the curve somewhat, it was not significantly different from the previous iteration.

C. IEEE Std 1031-2007 and Std 1361-2003

Both of these standards emphasize the importance of the battery capacity [6,7], which can be resolved by placing the PV series-array in parallel. The introduction of the circuit topology proposed and examined here offers a practical benefit in terms of geographical placement of the each array. That is, because the amount of cells required to obtain a desired output voltage is reduced, placing the individual arrays at locations that optimizes its exposure to the sun will significantly improve the output current, in comparison to a non-boosted PV system which restricts itself to an adjacent configuration. This effectively improves both sun hours (SH) and system losses (SL), which affects the number of parallel-arrays by:

$$N_p = \frac{\text{Load parameters}}{(1 - SL) \times SH} \quad (4)$$

The expression above implies then that the total amount of PV cells required for the overall system with a boosting circuit is less than a traditional stand-alone system in order to meet the load requirements of the battery. One additional parameter to consider with the series-array is the voltage window. The voltage output of the boost converter can be adjusted according to the voltage window determined in Std 1031 of the load. The upper limit V_{max} cannot exceed the maximum gain at the maximum duty cycle, as that would risk undercharging of the battery. Taking this into consideration and to take advantage of the maximum attainable gain of 3.5V/V to minimize the count, the PV series-array should be computed as follows:

$$N_{S_actual} \approx V_{max} / 3.5 \times V_{mod} \quad (5)$$

The above (5) is a slight alteration of the previously similar expression (3). The rationale for using the full gain rather than its closest integer as employed earlier was for higher accuracy during assessments that utilizes these standards for evaluation. It is recommended that the battery capacity testing procedures proposed in Std 1361 be conducted in the future to observe capacity losses over time with the proposed system.

V. FUTURE DEVELOPMENTS

A. Design Improvement for Demonstration Model

Since this is only the first iteration of the project there is certain opportunity for improvement. A potential improvement could be powering the microcontroller primarily from the output of the boosting circuit instead of an external power source. This would allow the device to be more mobile.

Another possible development could be designing a custom microcontroller especially for integrated implementation. This could decrease power consumption, and make the overall circuit size smaller. Future groups could also further optimize the inductor and capacitor components to reduce parasitic capacitive and resistive effects, in addition to further reductions in metal trace dimensions of the PCB. Testing could also been done at higher frequencies which again would reduce the capacitive effects [8]. This would require a processor that

could run at much higher frequencies than the current one used. A higher operating frequency will also reduce the inductance required for continuous current operations. This reduces the effective resistance of the reactive components, which in turn decreases power dissipation and can even slightly improve voltage amplification.

B. Applications

The most immediate application of the developments seen in this project will be the use of the device as a test bed for an integrated iteration.

With further exploration, the device could readily find use paired with a broad range of renewable energy sources, allowing for compaction and output specification. This project has explored such an application with the solar cell. A fully developed micro-circuit version of the boost converter could share the base substrate of the solar panel whose output it was meant to amplify. This will be particularly true in the integrated implementation wherein transparent materials may be utilized as composites for the active components [9]. It would then make it possible to apply the boosting circuit on the active face of the solar panel with limited performance loss. The widespread implementation of such coupled devices would result in a reduction in the surface area required to produce a desired potential difference.

VI. CONCLUSIONS

The project presented a functional demonstration model for DC-to-DC voltage boosting of a PV system. The PCB implementation achieved power efficiencies of over 45% at the expected input range, with a maximum gain of 3.5V/V at 68.5% duty cycle operating at 2MHz. Also demonstrated was the impact the introduction of a boost converter to a PV system would have on the three IEEE standards: 1013, 1361 and 1562. In particular, the reduction of the amount of both series (factor of three) and parallel cells required to achieve the desired power output. Demonstration model performance can be enhanced in terms of power efficiencies which can be achieved by adopting a higher operating frequency and further minimizing the dimensions of passive components including the metal traces of the PCB. This subsequently reduces the resistance of the reactive components, and resistive losses thus increasing power efficiency.

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